B3 cont'd C1 9-23. An electronic equipment comprising the electro-optical device according to claim 22.--

REMARKS

Claims 1-8 and 20-23 are pending. By this Amendment, claims 1 and 8 are amended, claims 9-19 are canceled and new claims 21-23 are added. Reconsideration in view of the above-amendments and following remarks is respectfully requested.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance (for the reasons discussed herein); (b) do not raise any new issue requiring further search and/or consideration (since the amendments amplify issues previously discussed throughout prosecution); (c) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (d) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because they are made in response to arguments raised in the final rejection. Entry of the amendments is thus respectfully requested.

The Office Action rejects to the drawings under 37 C.F.R. §1.83(a) because they fail to clearly show how the gate electrodes extend in both a width and length direction as described in the specification. Applicant amends Fig. 3 in the attached Request for Approval of Drawing Correction. Accordingly, Applicant respectfully request that the objection to the drawings be withdrawn.

The Office Action rejects claims 1 and 3-7 under 35 U.S.C. §102(b) as being anticipated by Nakazawa (U.S. Patent No. 5,614,730); claims 2 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakazawa, and further in view of ordinary skill

in the art; and claim 20 is rejected under 35 U.S.C. §103(a) as being unpatentable over Nakazawa, and further in view of Nishihara (Japanese Patent No. 06163891). Applicant respectfully traverses the rejection as applied to claims 1-8 and 20-23.

In particular, Applicant asserts that neither Nakazawa or Nishihara, alone or in combination, disclose or suggest an electro-optical device, including at least each of a plurality of transistors having a gate electrode and a semiconductor having a channel region and at least one portion extending outside of the channel region in a gate-width direction perpendicular to a gate-length direction that is a direction in which one of the plurality of data lines extends, the at least one portion and at least one of a source region and a drain region being separated by an extension of the gate electrode, and the extension extending in the gate-length direction outside of the semiconductor region, as recited in independent claim 1, and similarly recited in independent claim 8, 21 and 22.

Specifically, Nakazawa discloses a gate electrode extending in a gate width direction, which is a direction parallel with a scanning line 101, and extending in a gate length direction, which is a direction parallel with a date line 108. As shown in Fig. 19a of Nakazawa, only one end in the gate length direction of a gate electrode 103 extends outside of the semiconductor region forming the transistor. Accordingly, the lower end in the gate length direction of the gate electrode 103 does not extend outside of the gate line 113 in the semiconductor region.

Nishihara discloses in Figs. 7 and 8 portions of a scanning line 5 that form a gate electrode.

In stark contrast to Applicant's claimed invention, neither Nakazawa or Nishihara disclose or suggest an electro-optical device, including at least each of a plurality of transistors having a gate electrode and a semiconductor having a channel region and at least one portion extending outside of the channel region in a gate-width direction perpendicular to

a gate-length direction that is a direction in which one of the plurality of data lines extends, the at least one portion and at least one of a source region and a drain region being separated by an extension of the gate electrode, and the extension extending in the gate-length direction outside of the semiconductor region. Instead, the lower end in the gate length direction of the gate electrode 103 in Nakazawa does not extend outside of the gate line 113 in the semiconductor region.

Accordingly, because Nakazawa fails to disclose each and every feature as the claimed invention, Applicant asserts that independent claims 1, 21 and 22 define patentable subject matter. Claims 2-8 and 23 depend from the independent claims 1 and 22 and therefore also define patentable subject matter. Moreover, because Nishihara fails to compensate for deficiencies in Nakazawa, Applicant asserts that claim 20 defines patentable subject matter. Accordingly, Applicant respectfully request that the rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a) be withdrawn.

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1 - 8 and 20-23 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's attorney at the telephone number listed below.

Respectfully submitted,

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Registration No. 27,075

Richard S. Elias
Registration No. 48,806

JAO:RSE/alp

Attachments:
Appendix
Petition for Extension of Time
Request for Approval of Drawing Correction
w/Red Marked Fig. 3

Date: July 26, 2002

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APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claims:

1. (Amended) An electro-optical device, comprising:

a substrate;

a plurality of scanning lines ~~provide on the substrate~~;

a plurality of data lines, one of the data lines crossing one of the plurality of scanning lines; and

a plurality of transistors disposed correspondingly to intersections between the plurality of data lines and the plurality of scanning lines, ~~formed with gate electrodes having ends in a gate-width direction and ends in a gate-length direction, each transistor being connected to one of the scanning lines and one of the data lines; and~~

~~pixel electrodes connected to the transistors,~~

each of the plurality of transistors comprising:

a gate electrode; and

a semiconductor having a channel region and at least one portion extending outside of the channel region in a gate-width direction perpendicular to a gate-length direction that is a direction in which one of the plurality of data lines extends,

the at least one portion and at least one of a source region and a drain region being separated by an extension of the gate electrode, and the extension extending in the gate-length direction outside of the semiconductor region~~of the ends in the gate-width direction of the gate electrodes forming the transistors being disposed in a semiconductor region forming the transistor, and the ends in the gate-length direction of each of the gate electrodes extending outside of the semiconductor region forming the transistor~~.

8. (Amended) An ~~electro-optical device~~electronic equipment, comprising:

a light source;

the electro-optical device according to claim 1 that modulates, in accordance with image information, an incident light emitted by the light source; and

a projection system that projects a light modulated by the electro-optical device.

~~a substrate;~~

~~a plurality of scanning lines provided on the substrate;~~

~~a plurality of data lines crossing the plurality of scanning lines;~~

~~a plurality of transistors formed with gate electrodes having ends in a gate width direction and ends in a gate length direction, each transistor being connected to one of the scanning lines and one of the data lines; and~~

~~pixel electrodes connected to the transistors,~~

~~at least one portion of the ends in the gate width direction of each of gate electrodes forming the transistors being disposed in a semiconductor region forming the transistor, the ends in the gate length direction of each of the gate electrodes extending outside of the semiconductor region forming the transistor, and at least one of the ends in the gate width direction of a channel region of each transistor being electrically connectable.~~